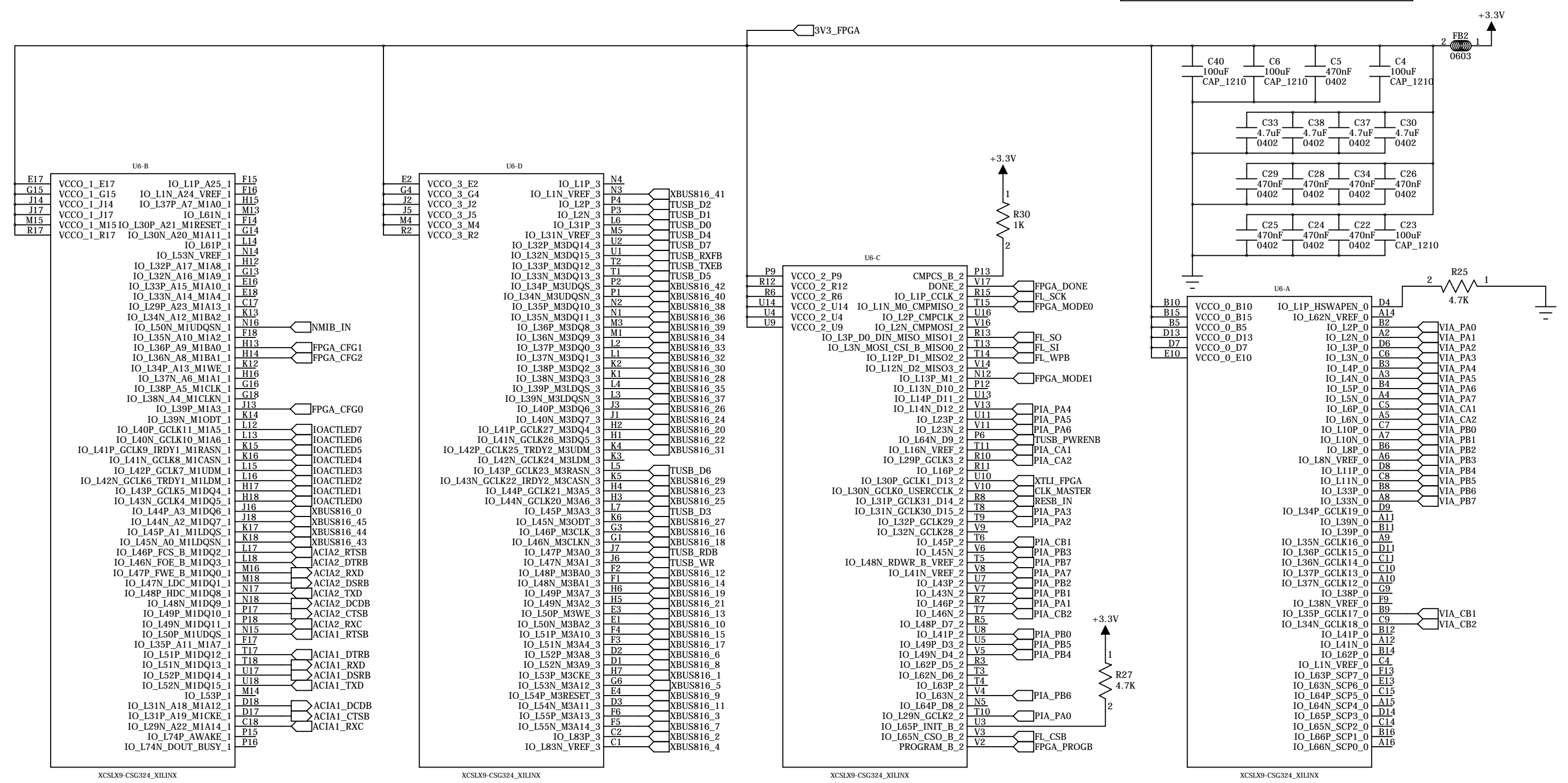
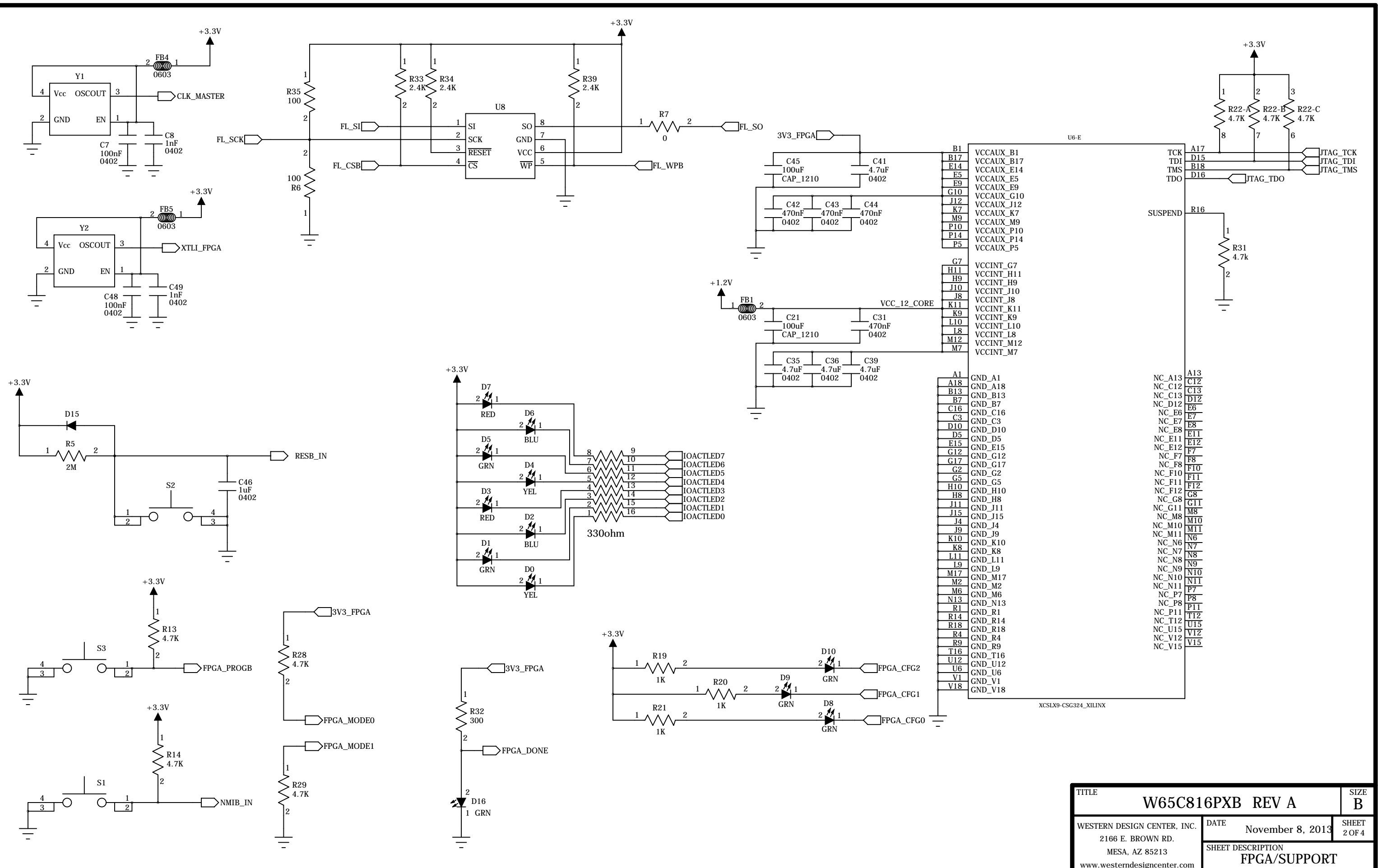


Place a 100uF cap on each side of FPGA on top
 Place a 4.7uF near each bank on the bottom
 Place 2 470nF near each bank on bottom

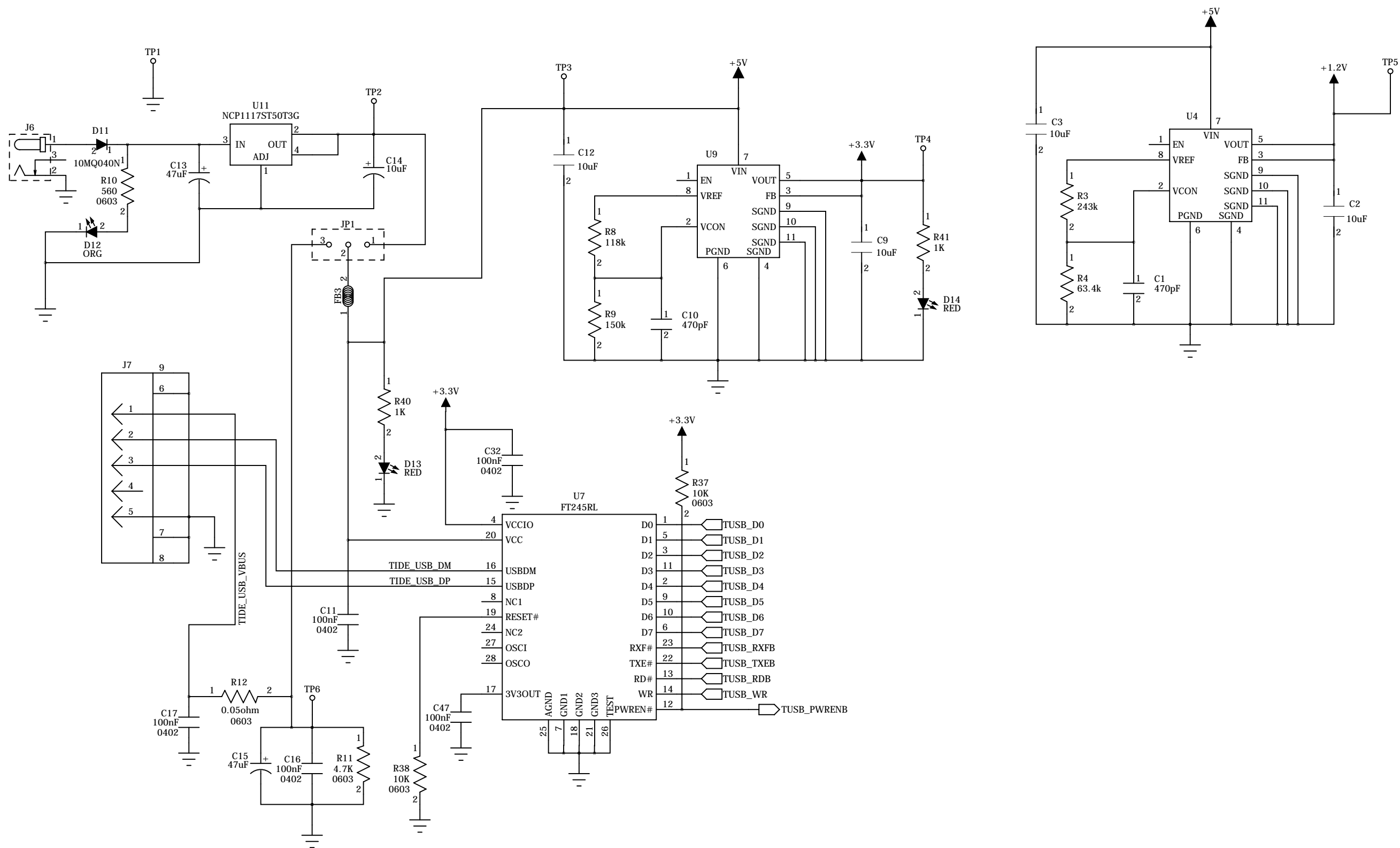


TITLE		W65C816PXB REV A		SIZE	B
WESTERN DESIGN CENTER, INC.		DATE	November 8, 2013	SHEET 1 OF 4	
2166 E. BROWN RD.		SHEET DESCRIPTION		FPGA	
MESA, AZ 85213		www.westerndesigncenter.com			

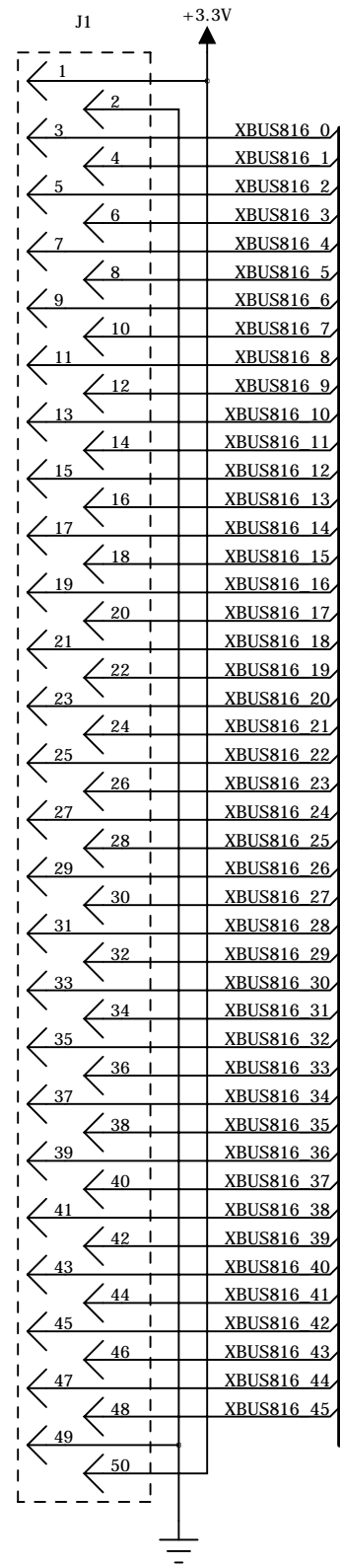


TITLE		W65C816PXB REV A		SIZE	B
WESTERN DESIGN CENTER, INC.		DATE	November 8, 2013	SHEET 2 OF 4	
2166 E. BROWN RD.		SHEET DESCRIPTION FPGA/SUPPORT			
MESA, AZ 85213					
www.westerndesigncenter.com					

TIDE_USB_DP/DM TO BE ROUTED AS A DIFFERENTIAL PAIR.

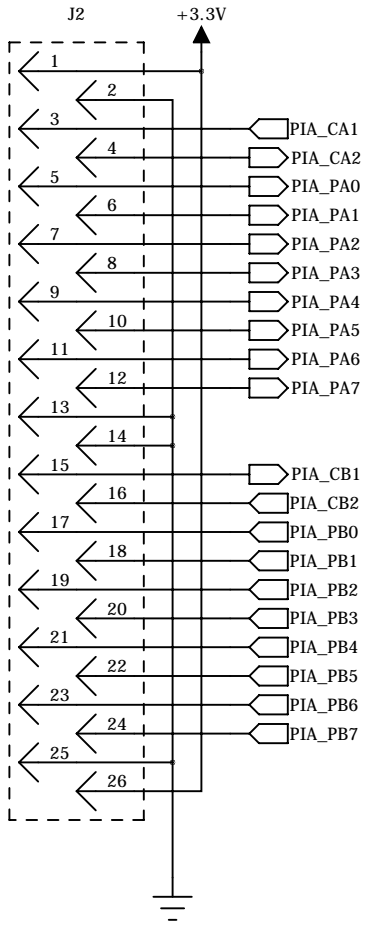


TITLE		W65C816PXB REV A		SIZE	B
WESTERN DESIGN CENTER, INC.		DATE	November 8, 2013	SHEET	
2166 E. BROWN RD.				3 OF 4	
MESA, AZ 85213		SHEET DESCRIPTION		TIDE USB INTERFACE	
www.westerndesigncenter.com					

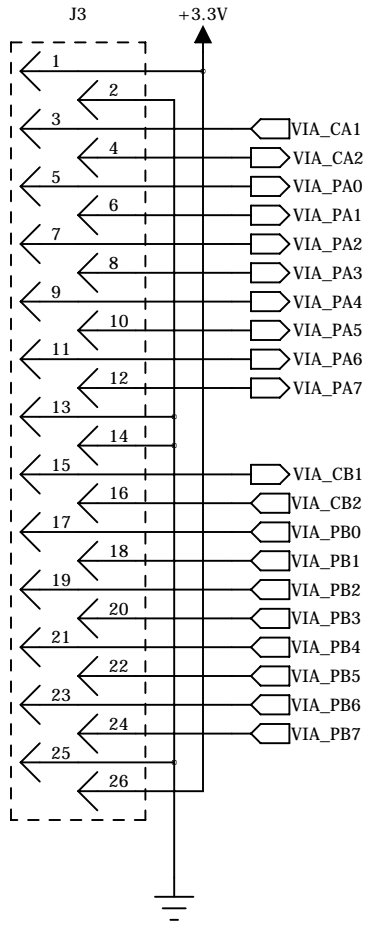


XBUS816_[0:45]

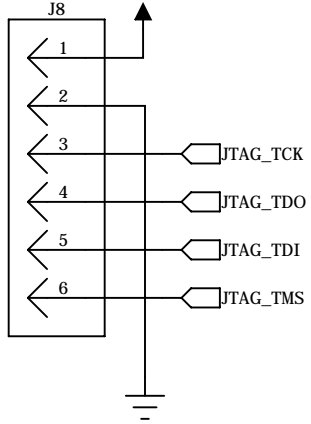
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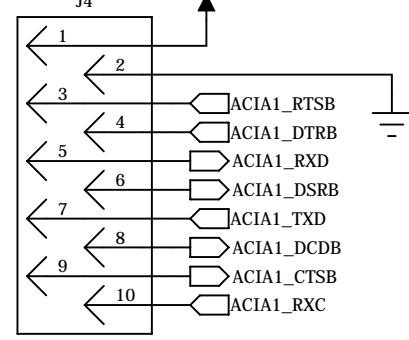
VIA_INT



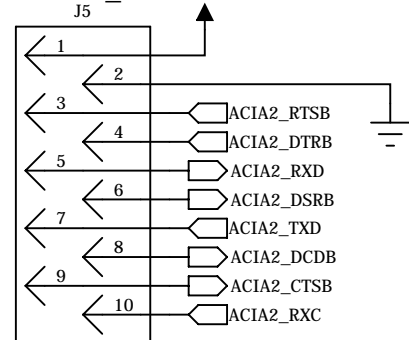
JTAG



ACIA1_INT



ACIA2_INT



TITLE		W65C816PXB REV A		SIZE	B
WESTERN DESIGN CENTER, INC. 2166 E. BROWN RD. MESA, AZ 85213 www.westerndesigncenter.com		DATE	November 8, 2013	SHEET 4 OF 4	
		SHEET DESCRIPTION CONNECTORS			